Amendments to Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Currently Amended) Architecture for controlling an electronic subsystem, comprising:

multiple integrated circuits, each having a plurality of input pins adapted to receive a parallel delivered signal adapted for controlling the corresponding integrated circuit; and

a single access port residing on one of the multiple integrated circuits, and adapted to receive a serial bit stream of data and convert the serial bit stream into the parallel delivered signal selectively placed onto the plurality of inputs pins of each of said multiple integrated circuits.

2. (Original) The architecture as recited in claim 1, wherein the serial bit stream is derived from a host computer operating from an application program compatible with IEEE Std. 1149.1.

3. (Original) The architecture as recited in claim 2, wherein the application program comprises the JAM™ Standard Test and Programming Language (STAPL).

4. (Canceled)

5. (Original) The architecture as recited in claim 1, wherein the access port comprises:

an instruction register coupled to receive the serial bit stream from a host computer;

a controller coupled to receive a clock signal and mode select signal from the host computer; and

a shift register coupled to receive the serial bit stream and convert the serial bit stream into the parallel delivered signal dependent on the state of the clock signal and mode select signal received upon the controller.

6. (Currently Amended) The architecture as recited in claim ~~1~~5, wherein the controller produces an enable signal upon ~~receive~~ receiving the clock signal and mode select signal compatible with IEEE Std. 1149.1.

7. (Currently Amended) The architecture as recited in claim ~~6~~5, wherein the shift register comprises any shift register within one ~~or more of said~~ of the multiple integrated circuits that can receive serialized data and place the serialized data upon the plurality of input pins dependent only on the state of the enable signal.

8. (Currently Amended) The architecture as recited in claim ~~6~~5, wherein clock signal and mode select signal are compatible with IEEE Std. 1149.1, and wherein the serialized data is incompatible with IEEE Std. 1149.1.

9. (Original) An access port coupled to receive a serial bit stream, and further coupled to receive control signals for controlling the serial bit stream in accordance with IEEE Std. 1149.1, the access port comprising:

a single controller coupled to receive the control signals and produce an enable signal dependent on the state of the control signals; and

a shift register within an integrated circuit absent circuitry compatible with IEEE Std. 1149.1, wherein the shift register is coupled to receive the serial bit stream and the enable signal for sending in parallel each bit of the serial bit stream onto a corresponding conductor of a plurality of conductors arranged upon the integrated circuit.

10. (Original) The access port as recited in claim 9, wherein the shift register is an encoder within an analog-to-digital converter.

11. (Original) The access port as recited in claim 9, wherein the shift register is an encoder within a digital-to-analog converter.

12. (Original) The access port as recited in claim 9, wherein the shift register is any shift register within core logic of the integrated circuit.

13. (Original) The access port as recited in claim 9, wherein the shift register is coupled to send in parallel the serial bit stream onto the plurality of conductors during a first time and, during a second time, the shift register is further coupled to receive in parallel a plurality of signals from a respective second plurality of conductors arranged upon the integrated circuit.

14. (Original) The access port as recited in claim 13, further comprising:

a multiplexer; and

an instruction decoder coupled to decode an instruction within the serial bit stream and, dependent on the instruction, to instruct the multiplexer to send onto an output conductor the serial bit stream or the plurality of signals from the second plurality of conductors.

15. (Original) The access port as recited in claim 14, wherein the control signals comprises a clock signal and a mode select signal.

16. (Original) The access port as recited in claim 9, further comprising:

a host computer coupled to the access port; and

four conductors extending between the host computer and the access port, wherein three of said four conductors are adapted to transfer the serial bit stream, the clock signal and mode select signal, respectively, to the access port from the host computer, and one of said four conductors is the output conductor.

17. (Original) A method for controlling input to and from a plurality of conductors arranged upon at least one integrated circuit, comprising:

sending control signals compliant with IEEE Std. 1149.1 onto a controller; and

depending on the status of the control signals, sending an enable signal from the controller to enable a shift register that is non-complaint with IEEE Std. 1149.1 to receive a serial bit stream and placing each bit of the serial bit stream upon corresponding ones of the plurality of conductors during a first time.

18. (Original) The method as recited in claim 17, further comprising receiving a parallel set of bits from corresponding ones of the plurality of conductors during a second time and converting the parallel set of bits into a second serial bit stream.

19. (Original) The method as recited in claim 18, further comprising, depending on an instruction within the serial bit stream, either placing the serial bit stream or the second serial bit stream upon an output conductor extending from the integrated circuit to a host computer.

20. (Original) The method as recited in claim 17, wherein said sending control signals comprises sending a Joint Test Action Group (JTAG) complaint clock signal and a test mode signal.